Investigating Portability in Chapel for Tree-based Optimization on GPU-powered Clusters

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IMEC - Leuven[1], Hewlett Packard Enterprise[2], University of Luxembourg[3], University of Lille[3 4]

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Outline

- Context, motivations and objectives
- Distributed Tree-based Search in Chapel
- The Complexity of Mixing CUDA/HIP with Chapel
- Performance Portability Experiments
- Performance Portability Results
- Programming Effort
- Conclusions and Perspectives

Introduction

Context, motivations and objectives

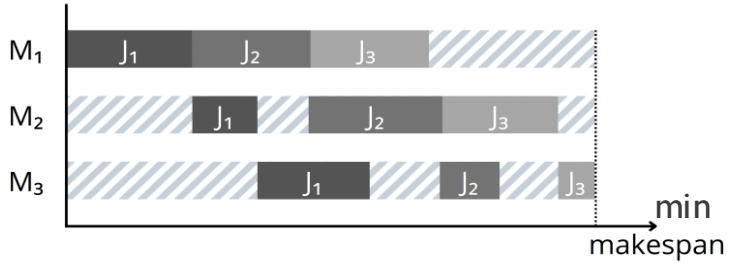
Context and motivations

Combinatorial Optimization Problems

- Optimization problems are increasingly big in many application areas
  - High-dimensionality (#decision variables, #objectives)
  - Time-demanding objectives

$$(O.P) \begin{cases} \min f(x) = (f_1(x), f_2(x), \ldots, f_n(x)) \\ \textbf{s.t.} \quad x \in S \end{cases}$$

- **Motivating Example:** Flow-shop scheduling problem
  - Big instance Ta056 (50 jobs, 20 machines) 10^64 sub-problems
  - 22 years using a single-core processor [M. Mezmaz et al., 2006]
  - **We do need supercomputers to solve big COPs!**



Context and motivations (cont.)

Tree-based Search Algorithms – Branch-and-Bound and Backtracking

- 4 Operators:
  - Branching
  - Bounding
  - Pruning and Selection (DFS, BFS,…)
- Major properties:
  - Huge tree
  - Very dynamic and irregular loads
  - Load balancing is required

Context and motivations (cont.)

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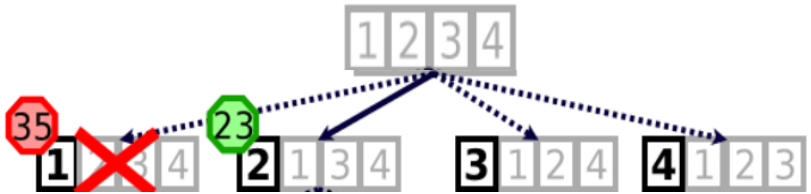

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Branching

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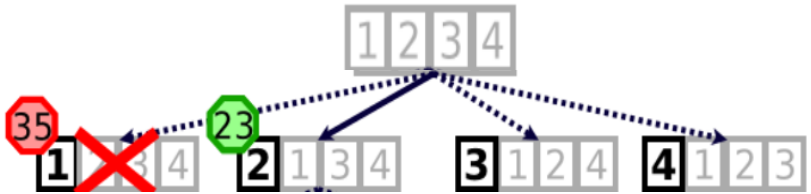

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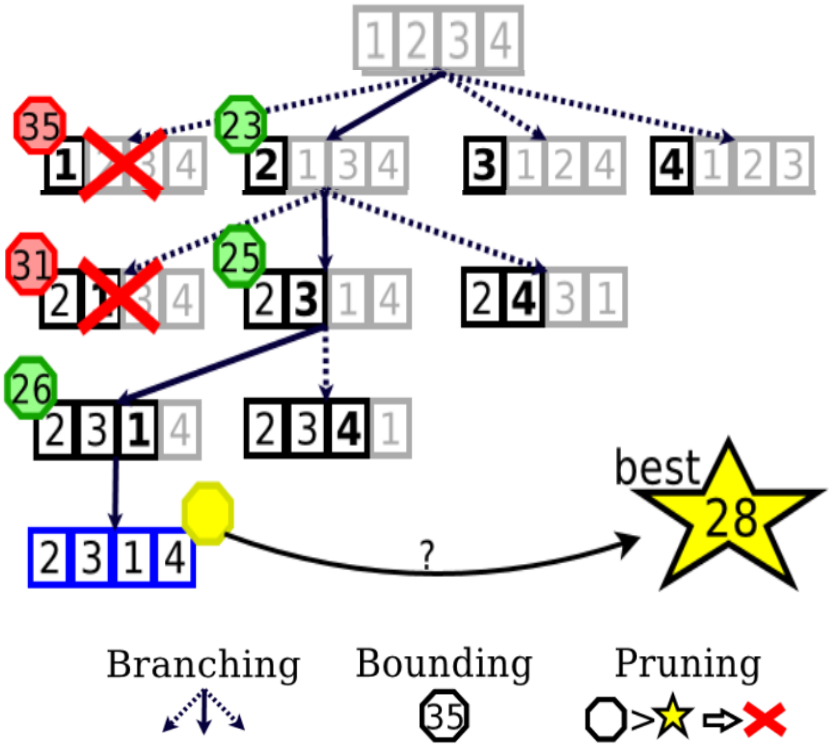

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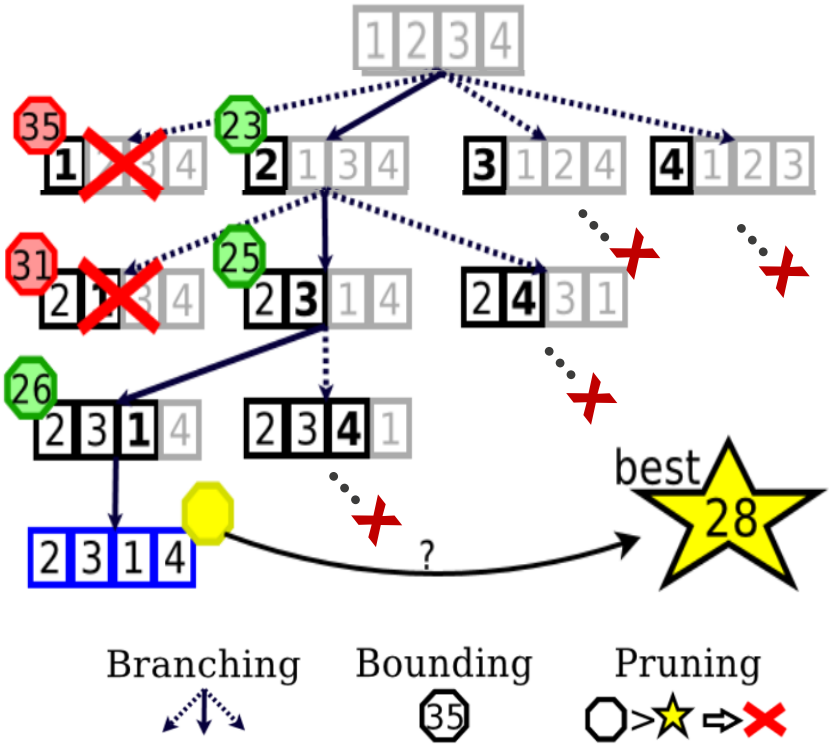

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Productivity-aware Ultra-scale Optimization

- Revisit the design and implementation of parallel tree-based search for solving COPs on large-scale supercomputers dealing with …
  - Productivity awareness
  - Parallel efficiency

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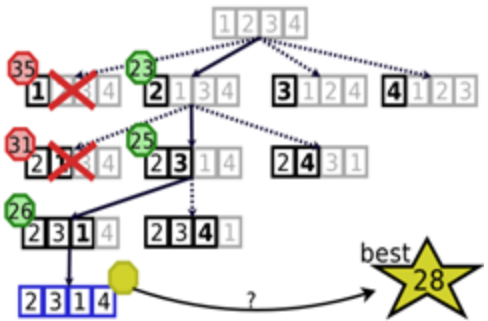

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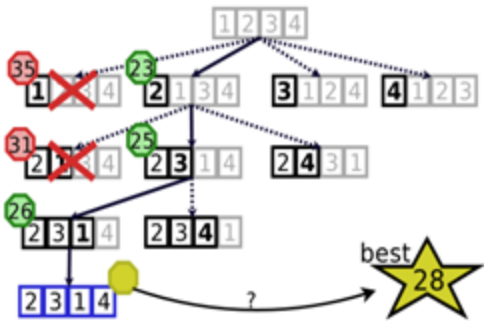

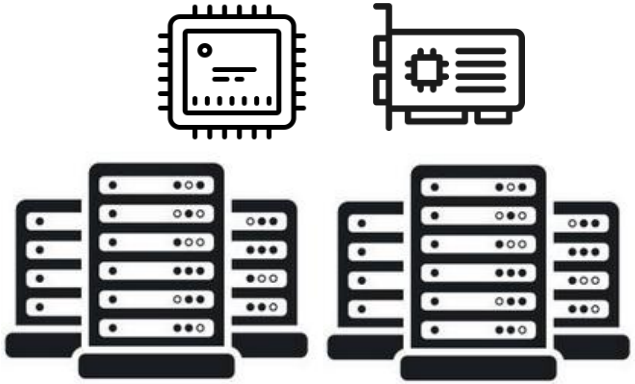

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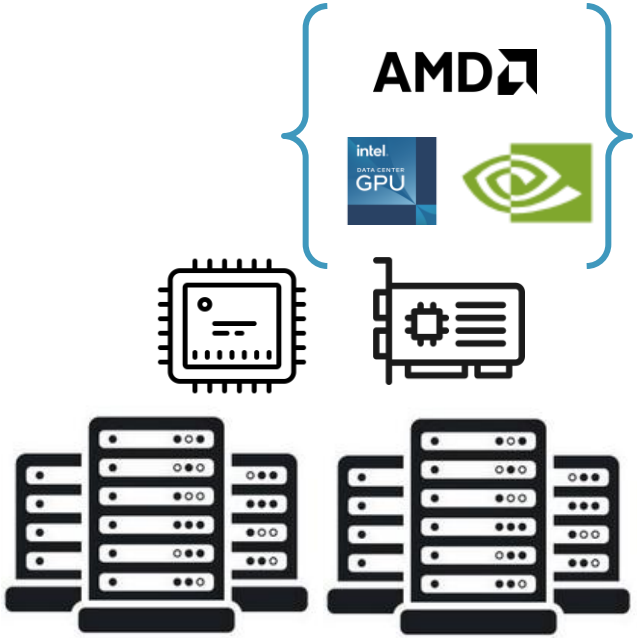
  - **Code and performance portability**



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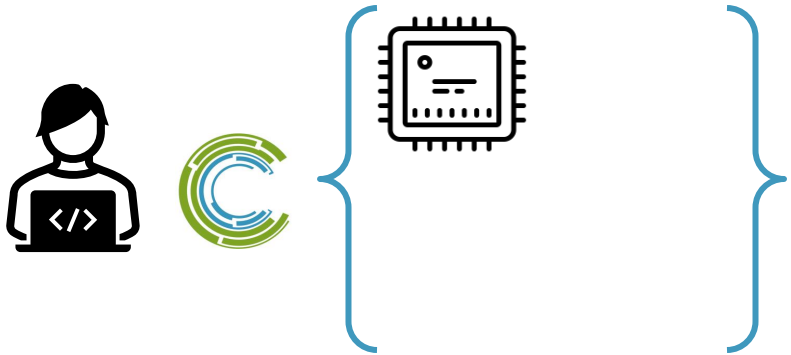

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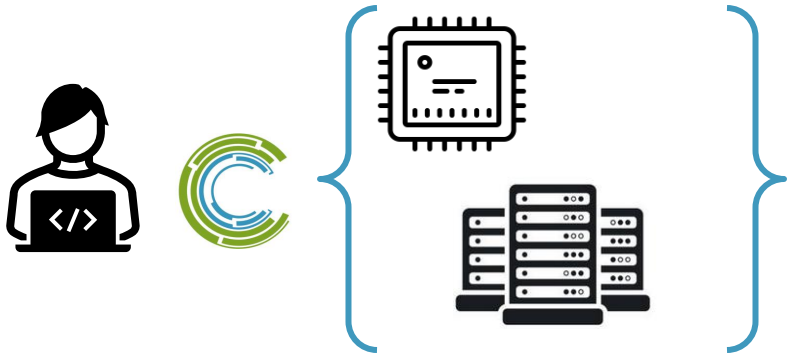

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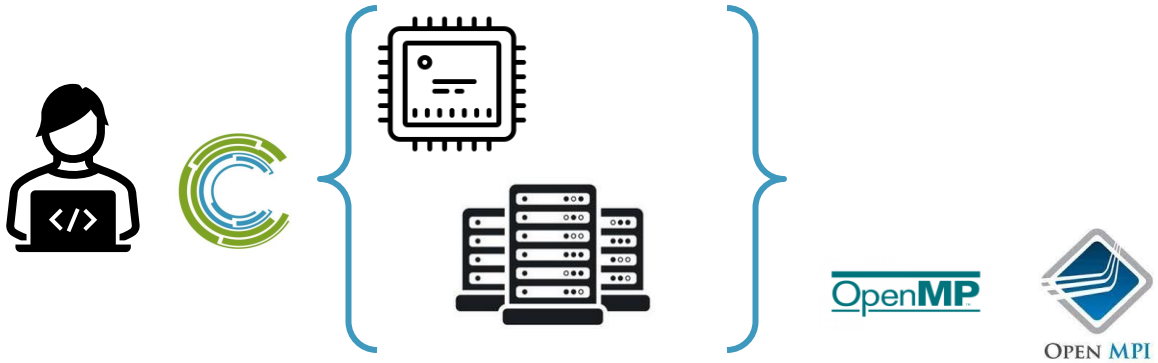

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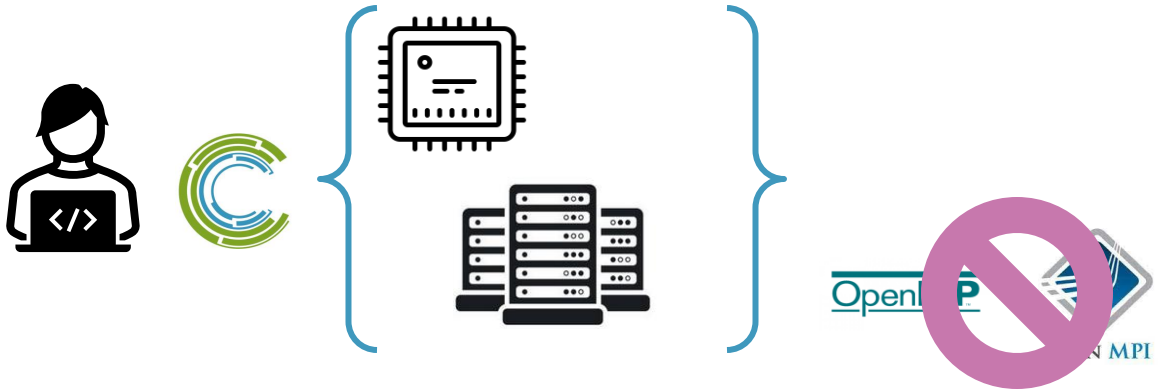

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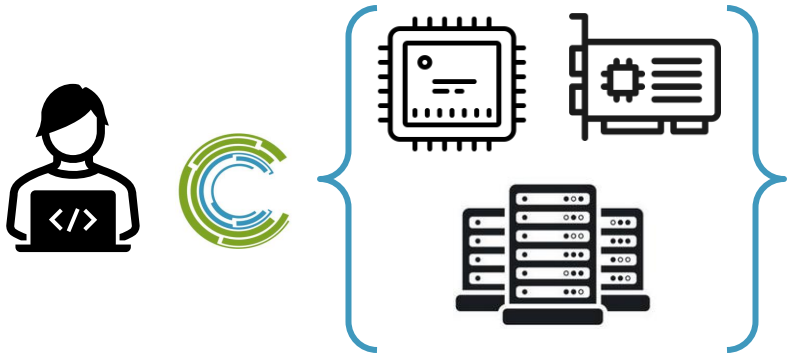

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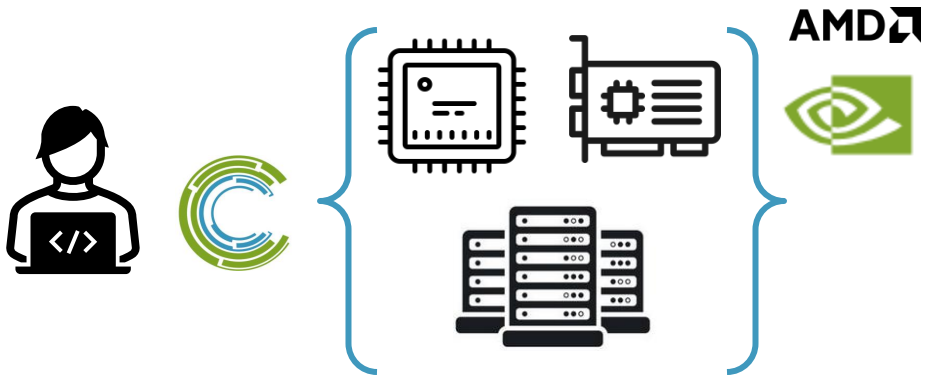

Distributed Tree-based Search in Chapel

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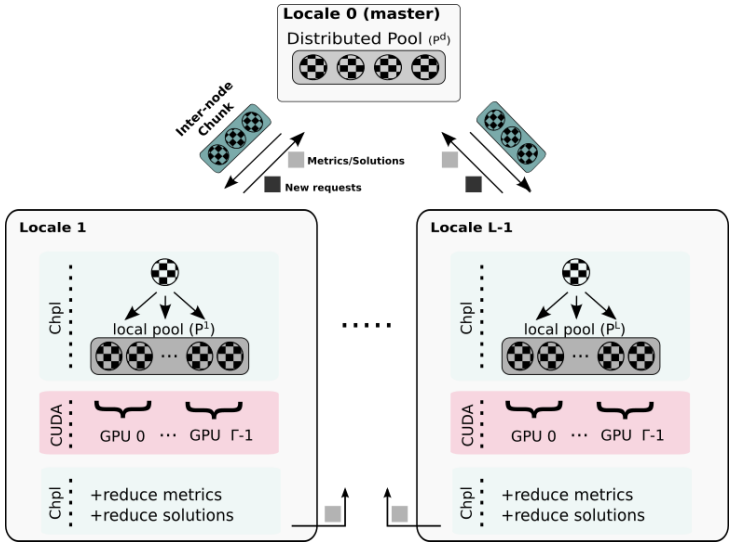

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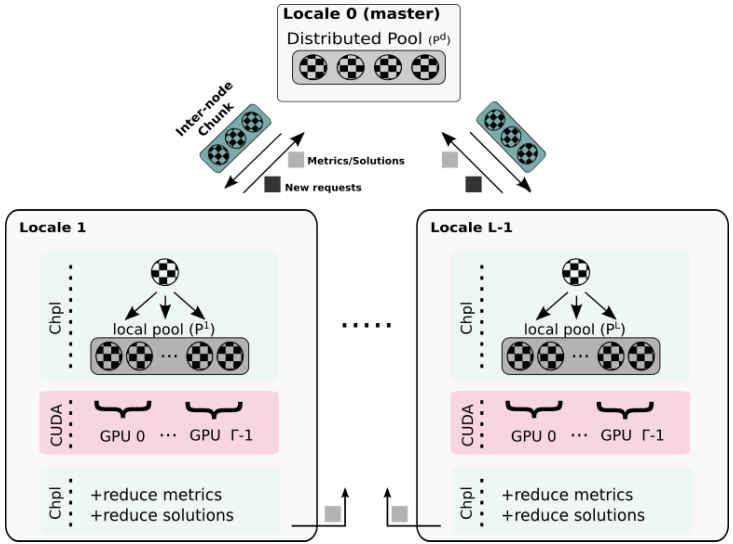

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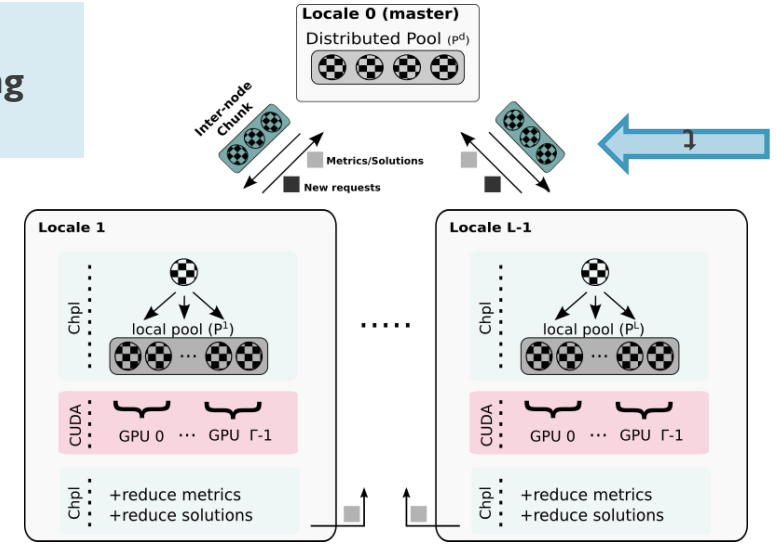

DistributedIters:
distributed load balancing/work distribution
Metrics reduction
Termination criteria

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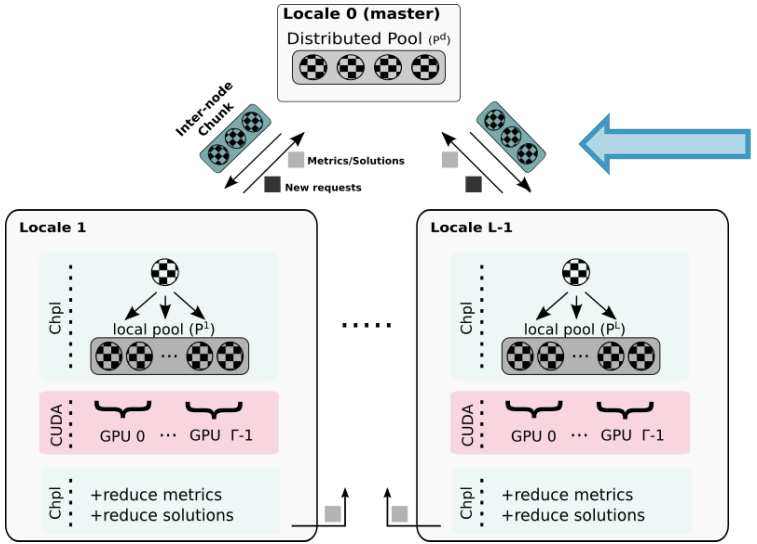
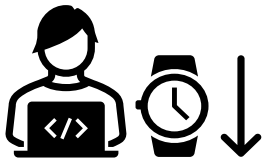


DistributedIters:
Increases productivity in the context of distributed tree-based search!



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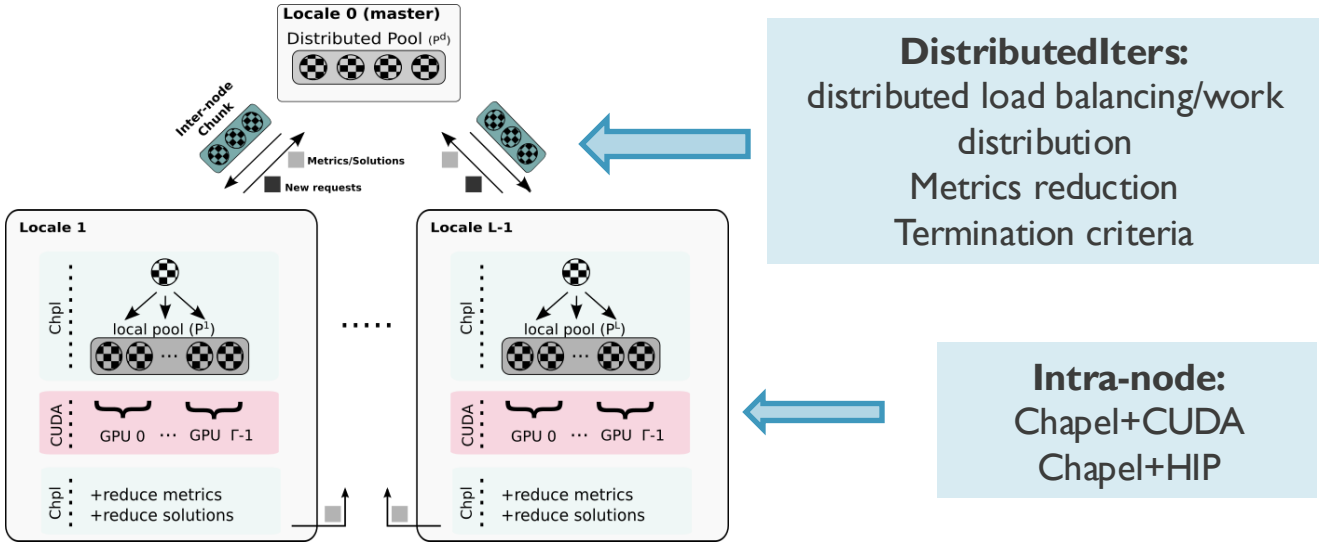

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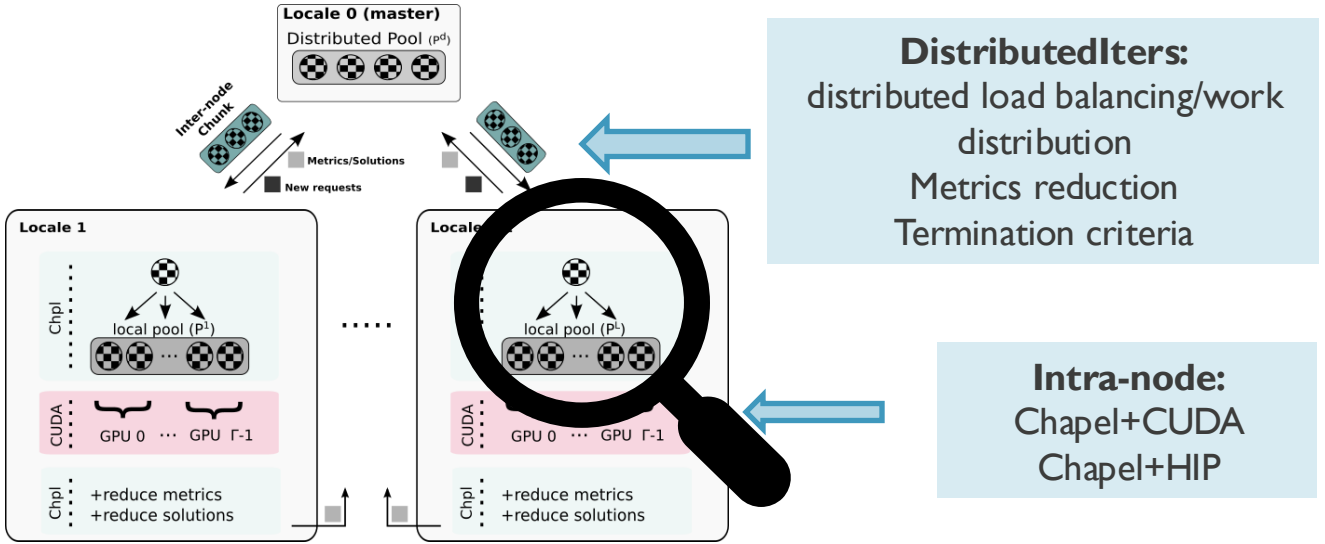

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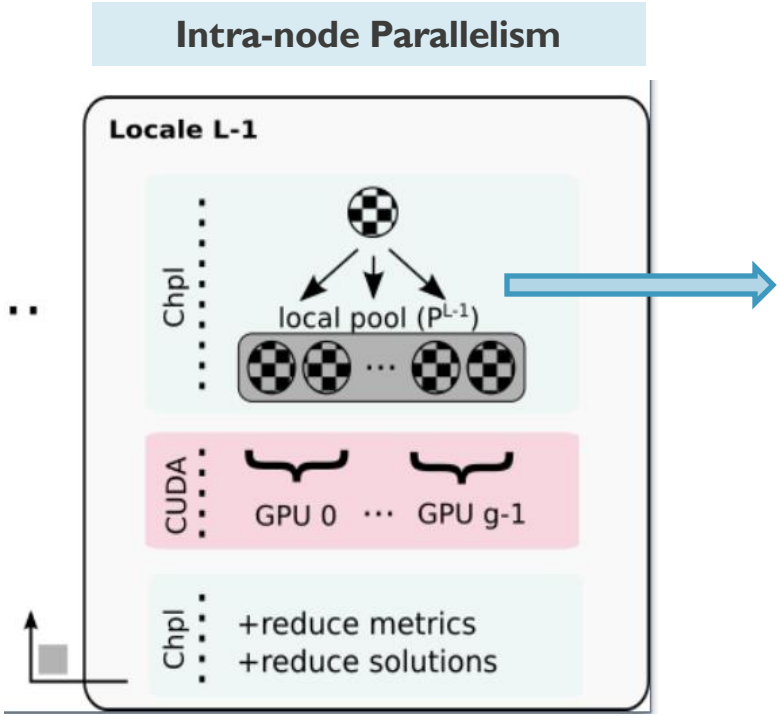
The Complexity of Mixing CUDA/HIP with Chapel

The Complexity of Using C-Interoperability

Mix of Programming Languages and Programming Models



From a subproblem in the chunk:
Generates load for the GPUs
Improves locality

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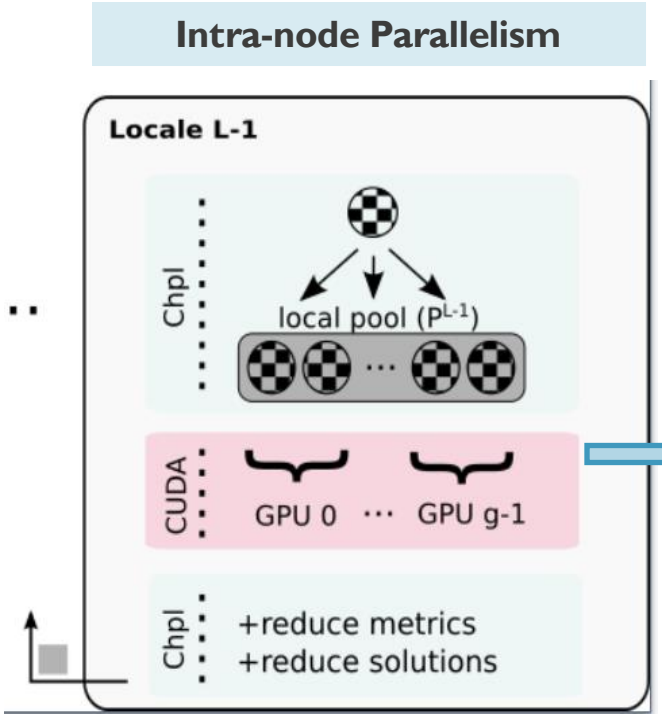
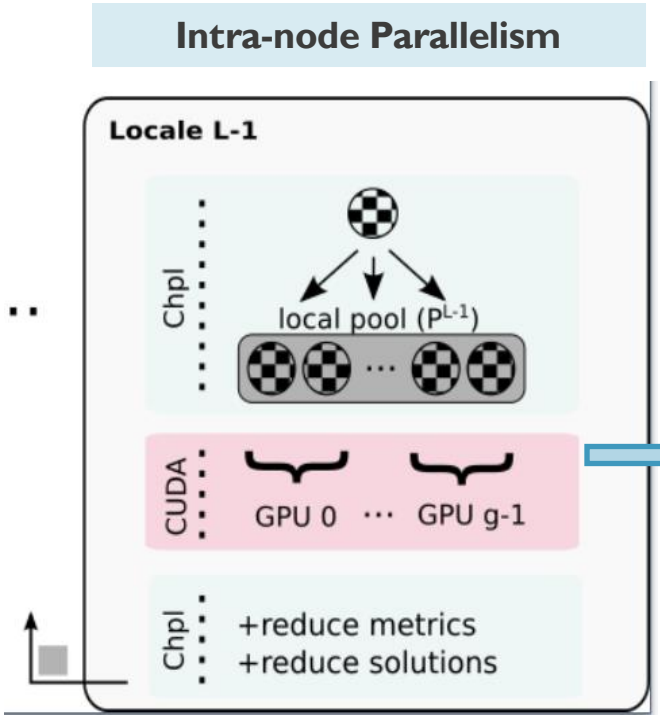


Calling the kernels and load distribution:
Tasks in Chapel – 1 task per GPU
C-Interoperability types and functions
(`c_ulonglong`, `CPtrTo(pool+chunk)`)

The Complexity of Using C-Interoperability

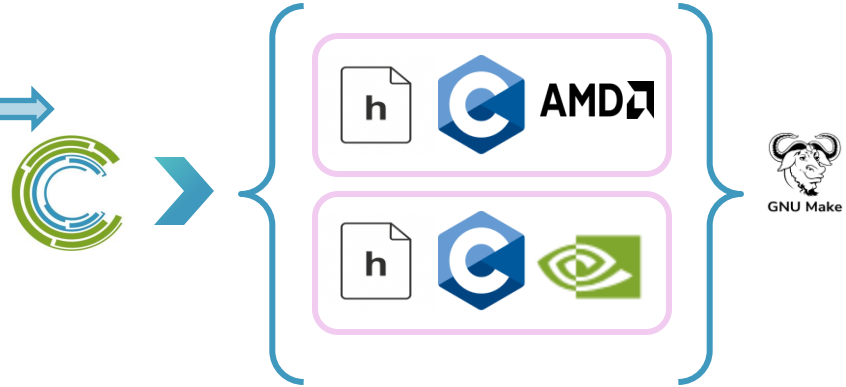
Redundant Kernel Implementations



Redundant kernels in CUDA and HIP

Wrapper function in C

Different Makefile rules



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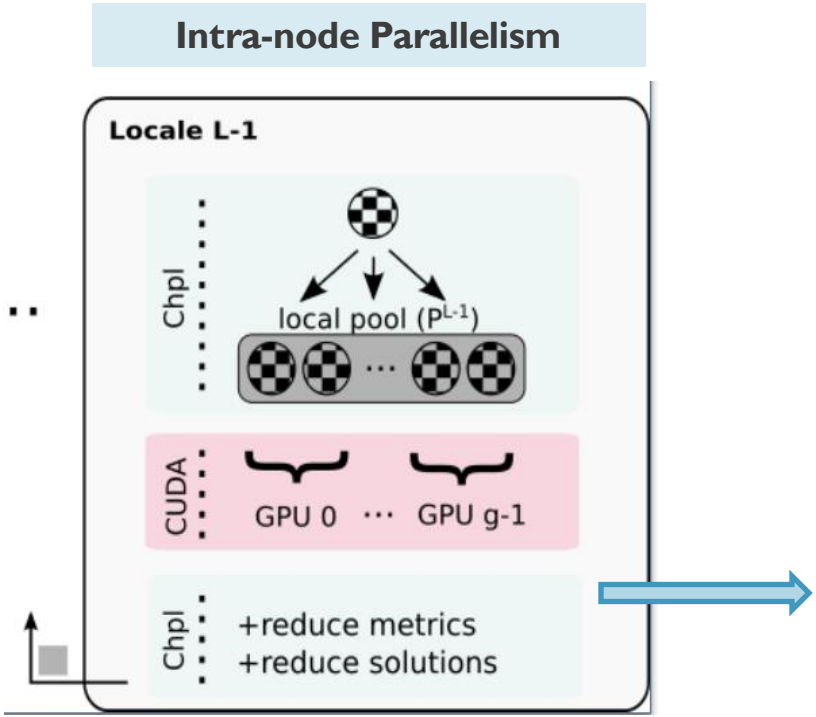
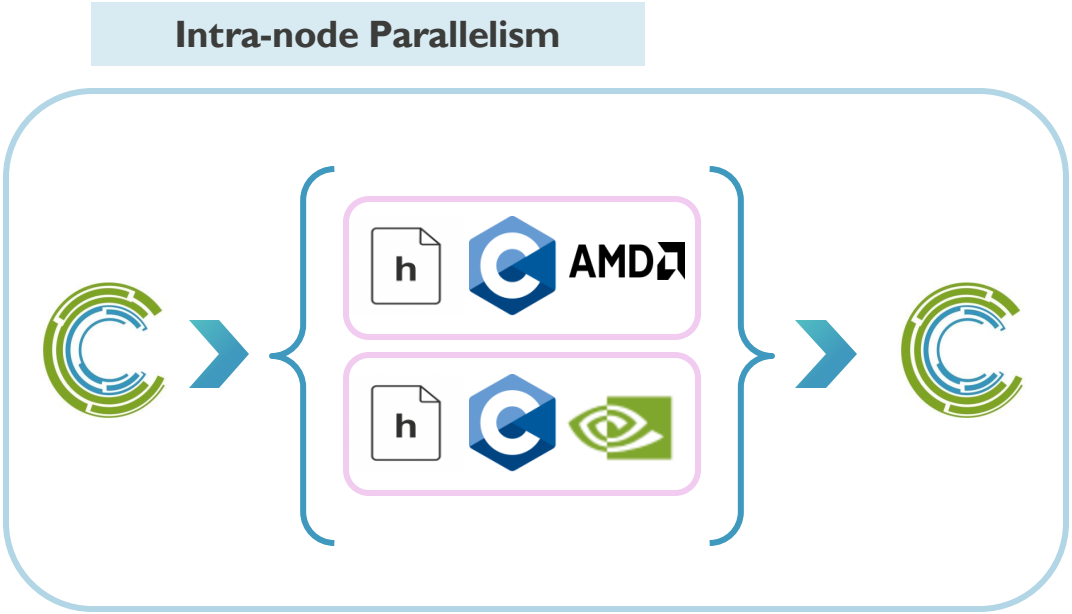


Gets the result back from the C-Wrapper

Uses C-Interoperability types

The Complexity of Using C-Interoperability

Programming Complexity and Productivity Loss



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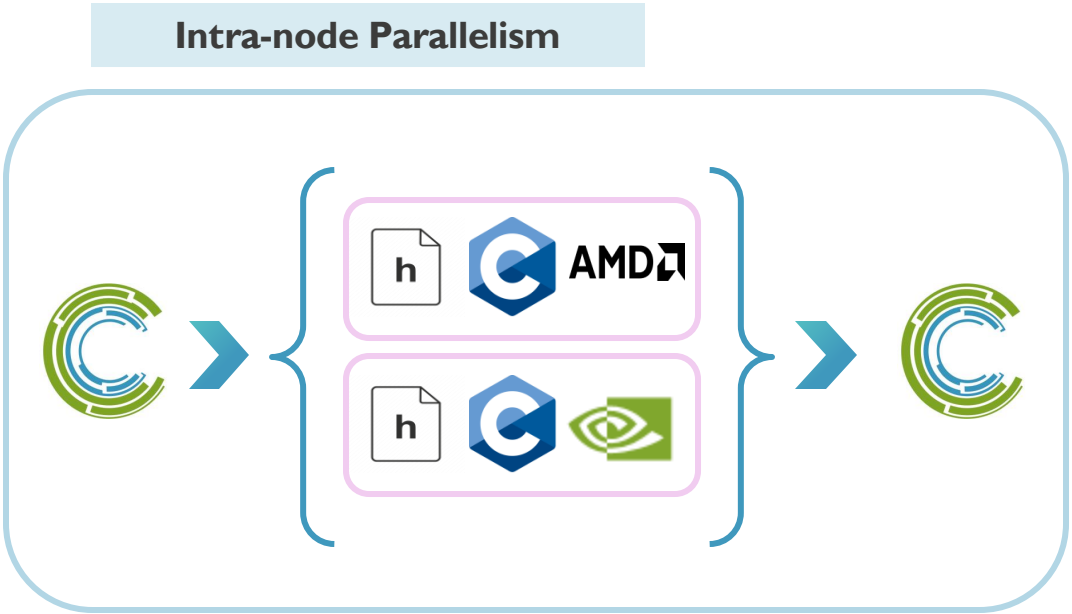

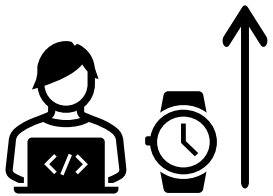

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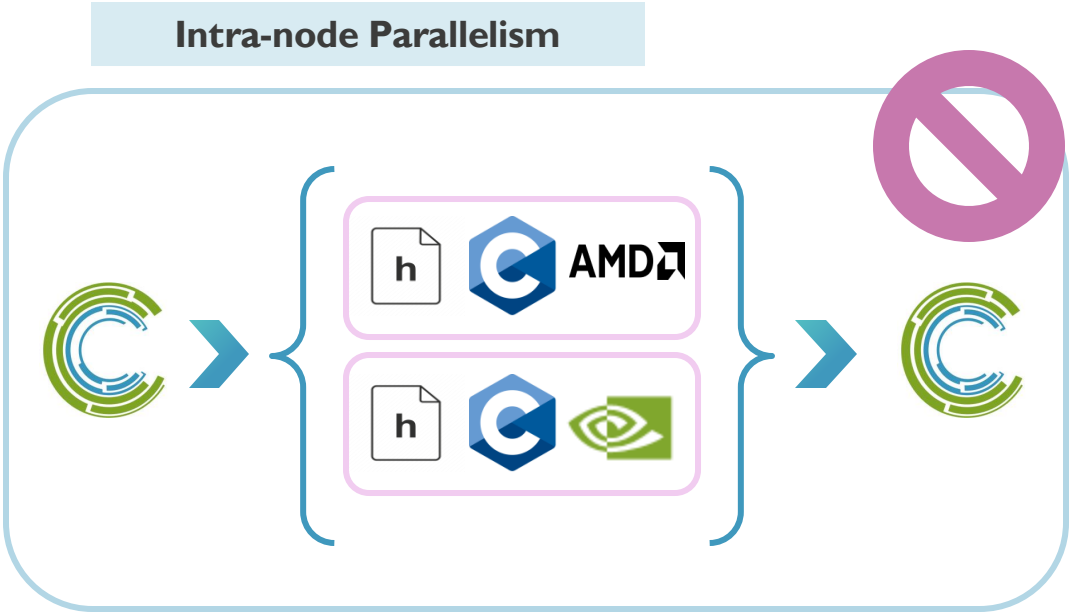

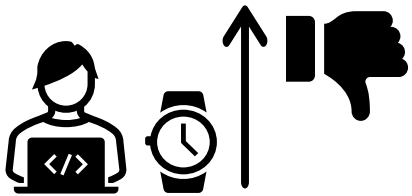

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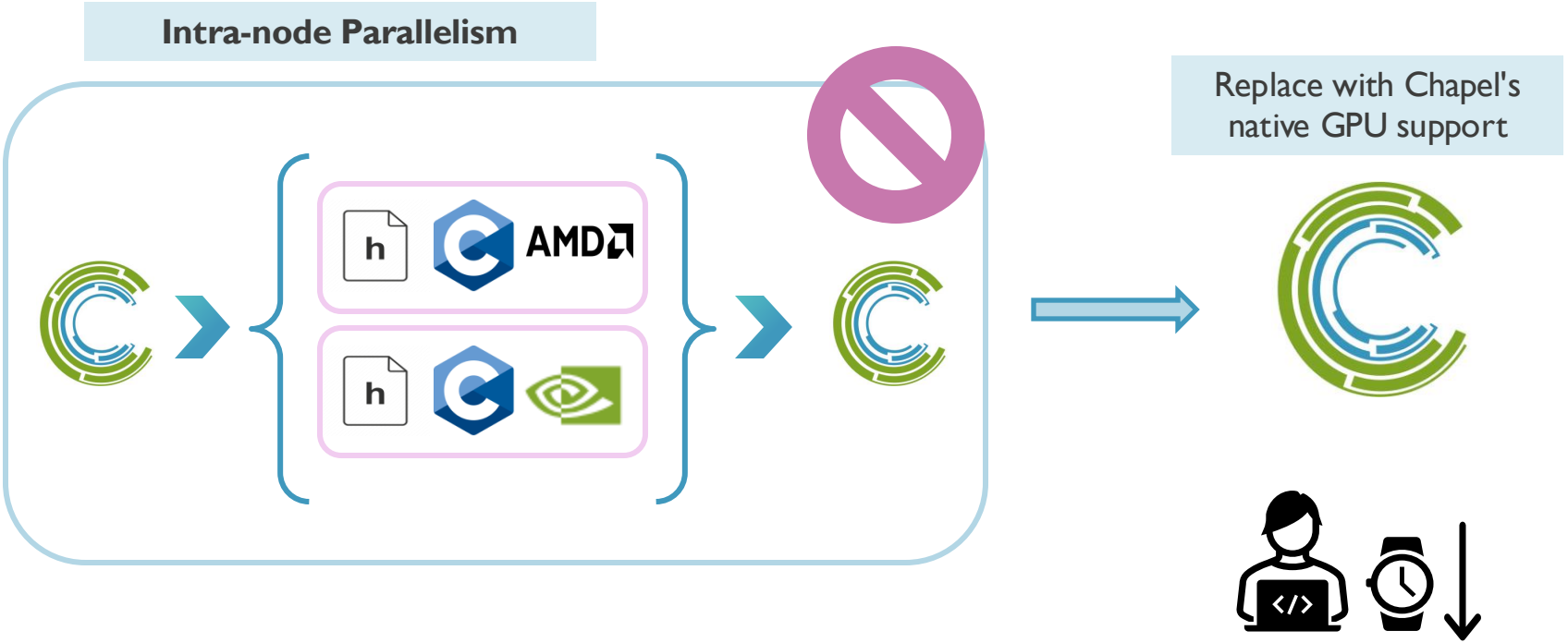

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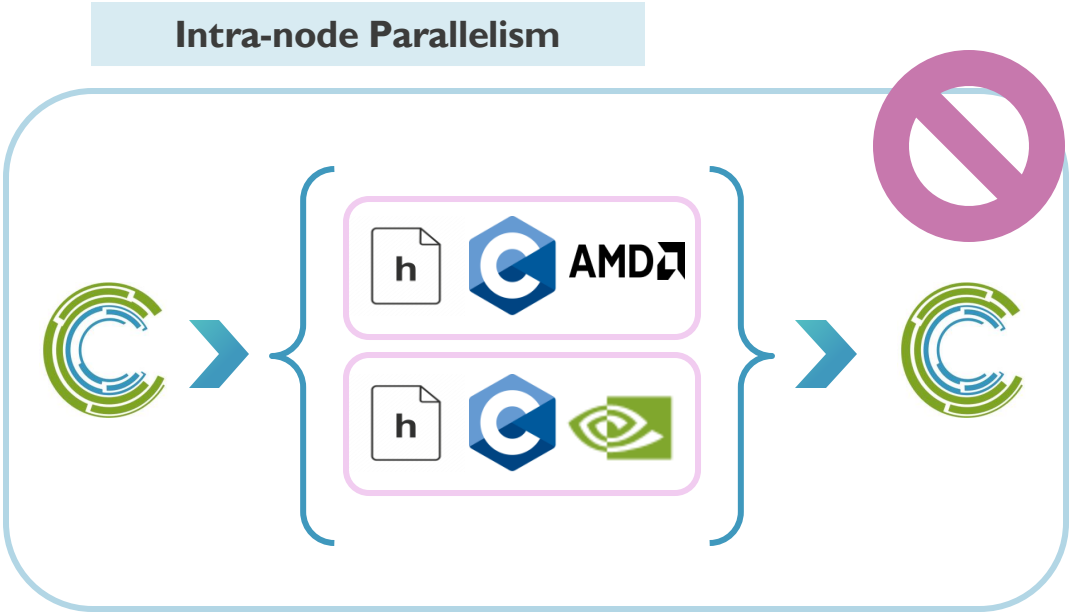

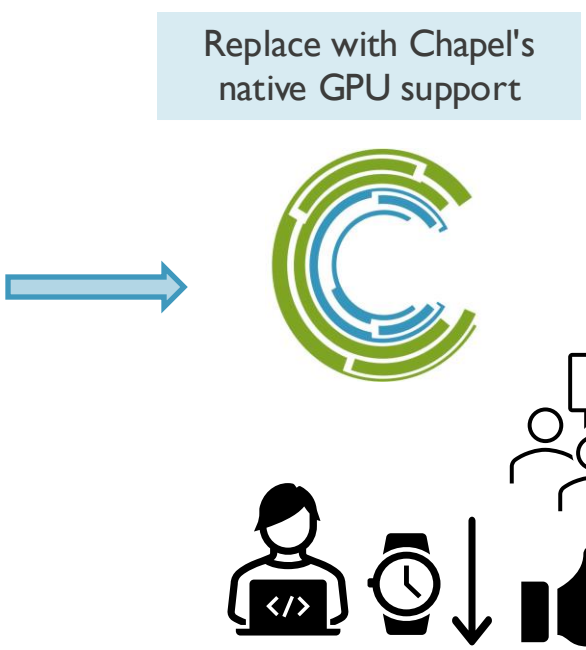

Research Questions

1. Is it possible to achieve both code and performance portability in distributed tree-based search with Chapel's native GPU support?
2. Is it worth in terms of programming effort?

Performance Experiments

Performance Experiments

Baselines

- The following applications for enumerating all valid complete solutions of the N-Queens problem are considered: (Backtracking)
  - **Single-node Multi-GPU *baselines*:** HIP+OpenMP **and** CUDA+OpenMP
  - **Single-node Multi-GPU:** Chapel-GPU
  - **Distributed Hybrid:** Chapel+CUDA **and** Chapel+HIP
  - **Distributed Chapel-GPU:** Chape's native GPU support

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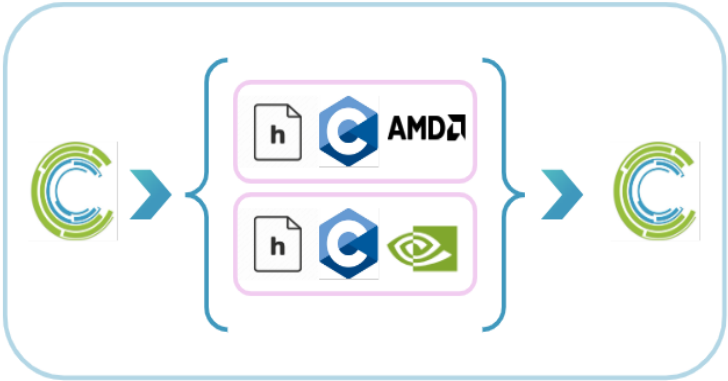

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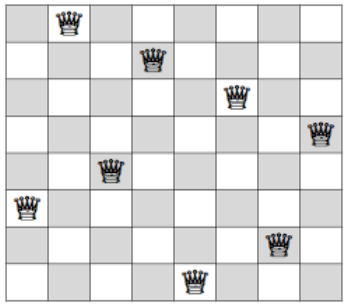

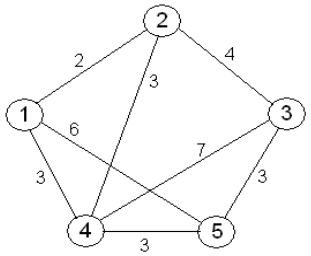

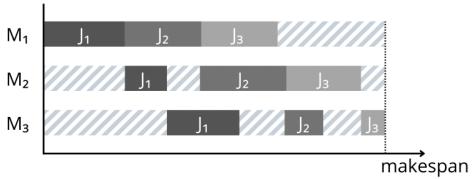

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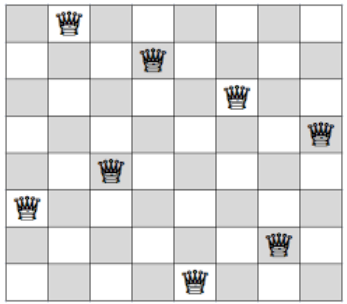
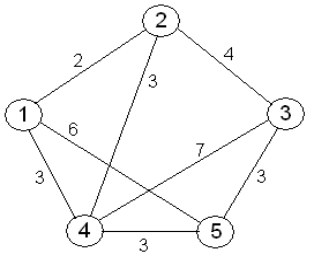
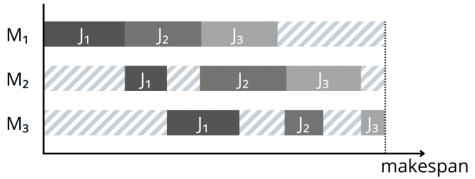


N-Queens – proof of concept

C. Optimization Problems – B&B





Performance Experiments

Testbeds and Parameters - Problems

- **N-Queens:**
  - Problem sizes (board) ranging from N=18 **to** N=22
    - **N=18:**
      - $6.6 * 10^{8}$ solutions
      - $2.96 * 10^{10}$ valid placements of queens on the board
    - **N=22**
      - $2.69 * 10^{12}$ solutions
      - $1.43 * 10^{14}$ valid placements of queens on the board
    - From ~10 seconds (N=18) to ~8 hours (N=22) on 8 GPUs.

Performance Experiments

Testbeds and Parameters - Computers

- NVIDIA System:
  - Perlmutter supercomputer (#14 of TOP500)
  - 1 to 128 computer nodes
  - 4 to 512 GPUs (A100 SXM4)
- AMD System:
  - Frontier supercomputer (#1 of TOP500)
  - 1 to 128 computer nodes
  - 8 to 1024 GPUs (MI250As)
  - (only two hours of execution)

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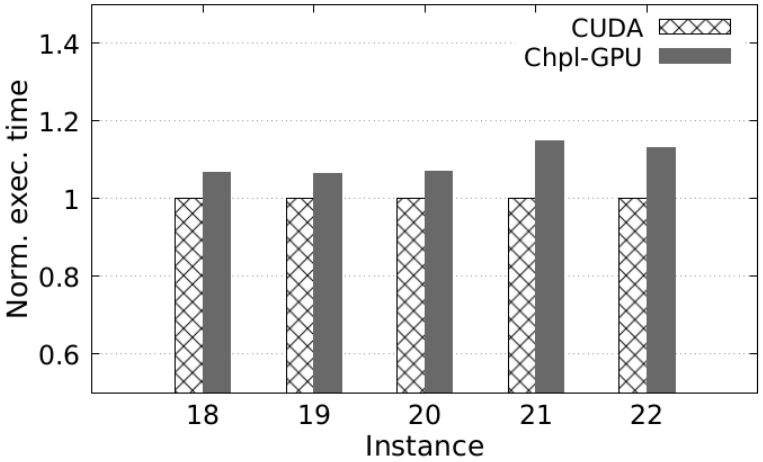
Performance Portability Results

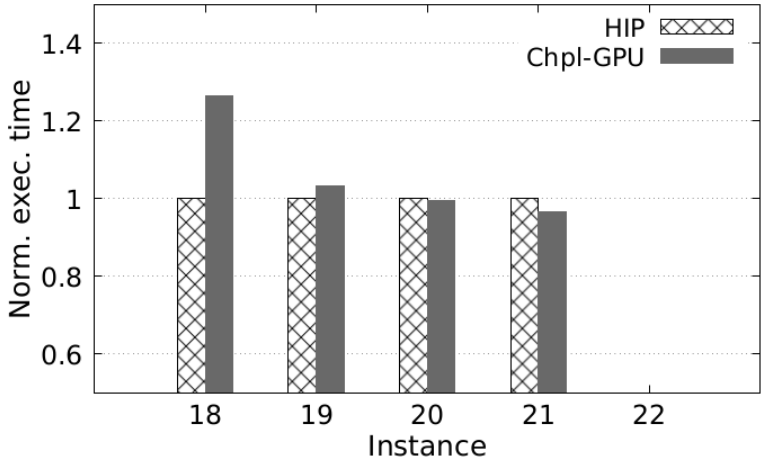
Performance Results

Single-node Application: execution time

- N-Queens of sizes ranging from N=18 to N=22
- 4 GPUS – NVIDIA, 8 GPUs – AMD, Chapel's native GPU support *vs.* Baseline



(a) vs. CUDA - NVIDIA-based System



(b) vs. HIP - AMD-based System

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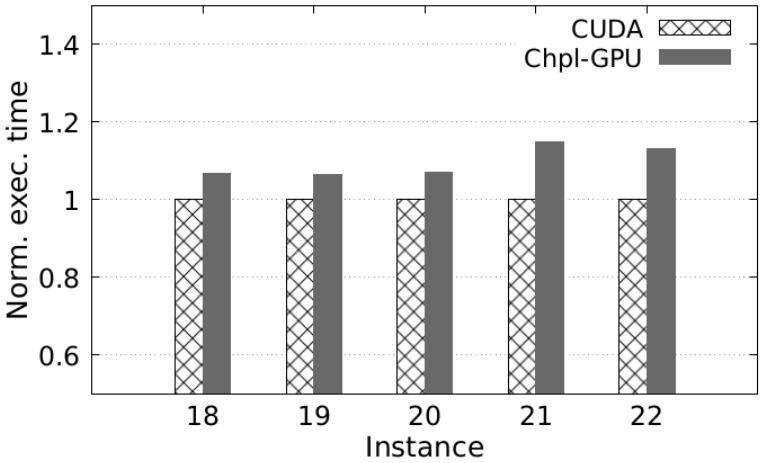

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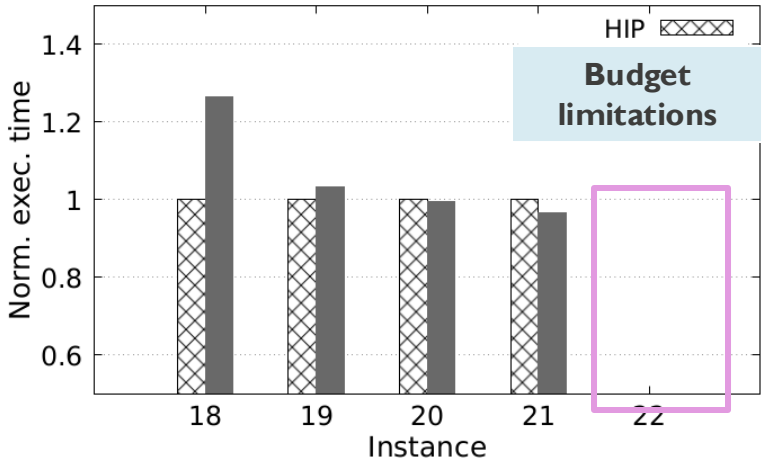

(b) vs. HIP - AMD-based System

Performance Results

Single-node Application: execution time

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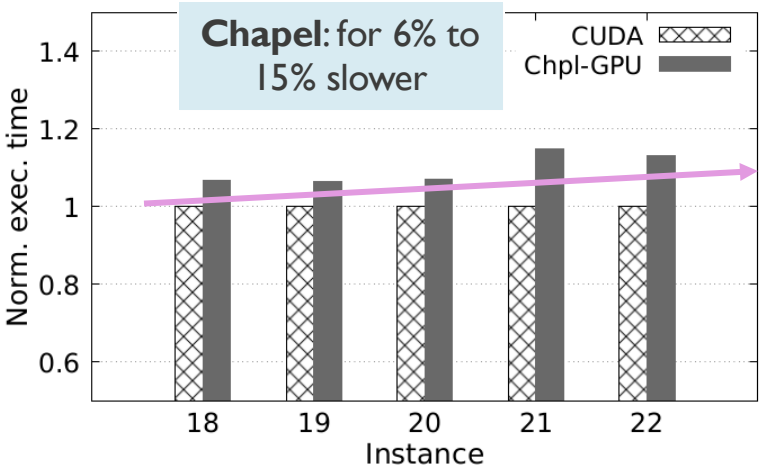
- 4 GPUS – NVIDIA, 8 GPUs - AMD

The **bigger** the load - the **better** the Chapel performance



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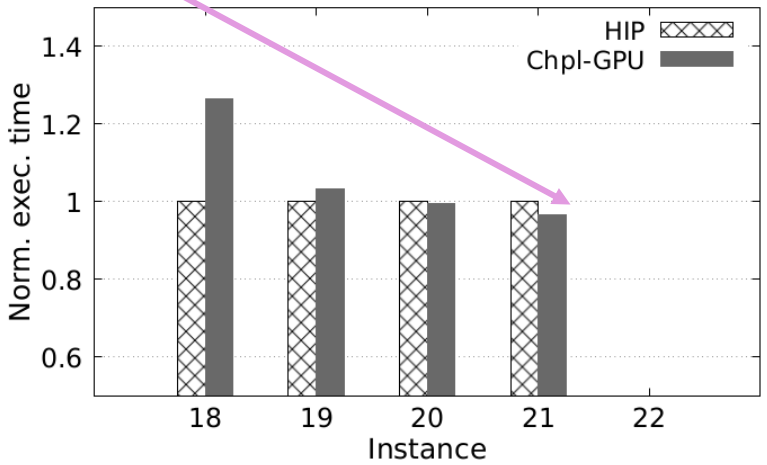
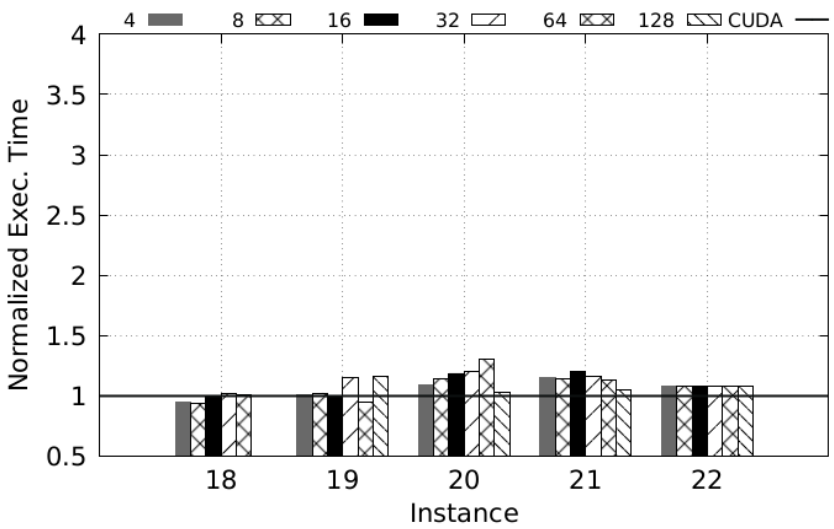


(b) vs. HIP - AMD-based System

Performance Results

Distributed Application: execution time

- N-Queens of sizes ranging from N=18 to N=22
- 4 to 128 computer nodes, Chapel's native GPU support *vs.* Hybrid



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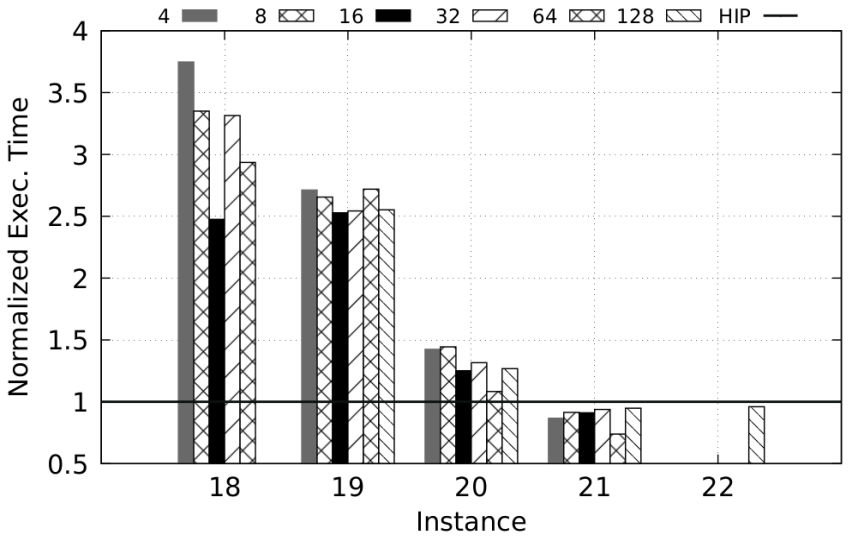

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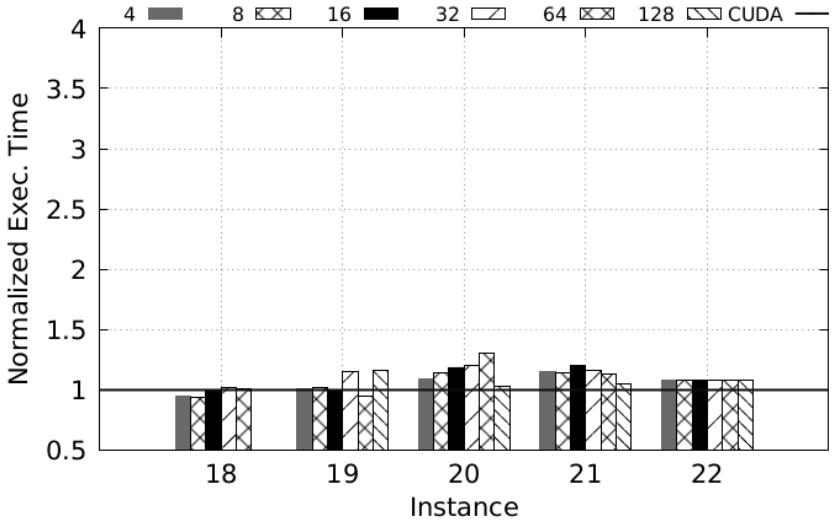

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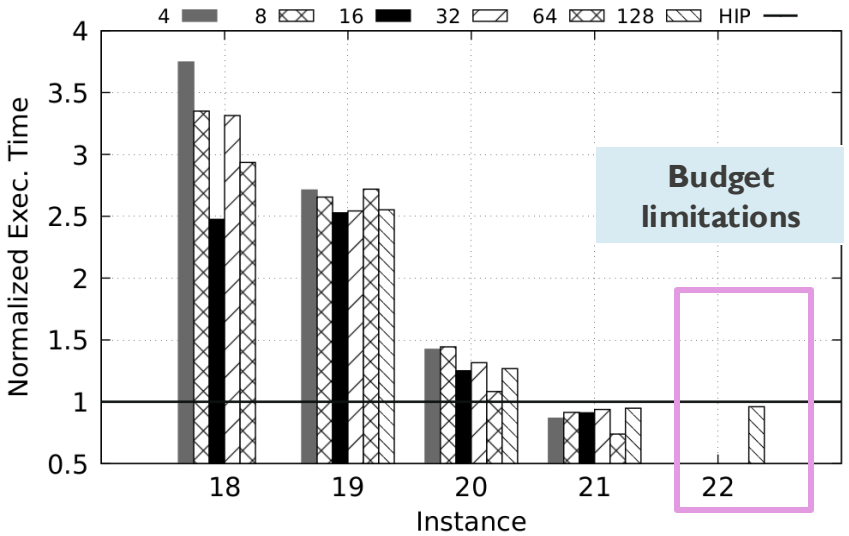

(b) vs. HIP - AMD-based System

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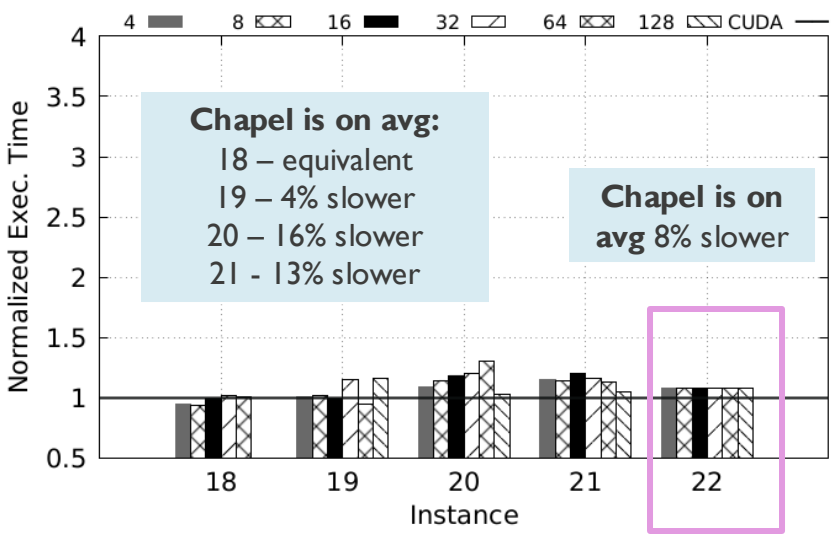

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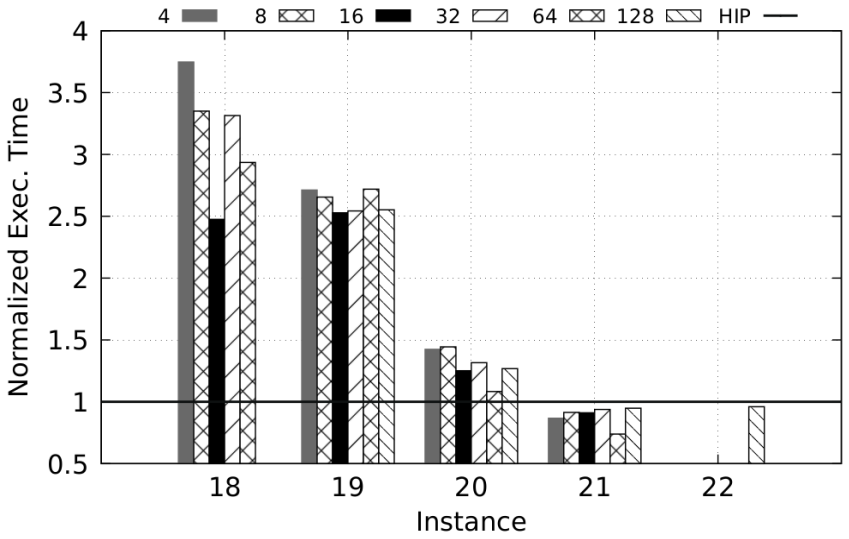

(b) vs. HIP - AMD-based System

imec

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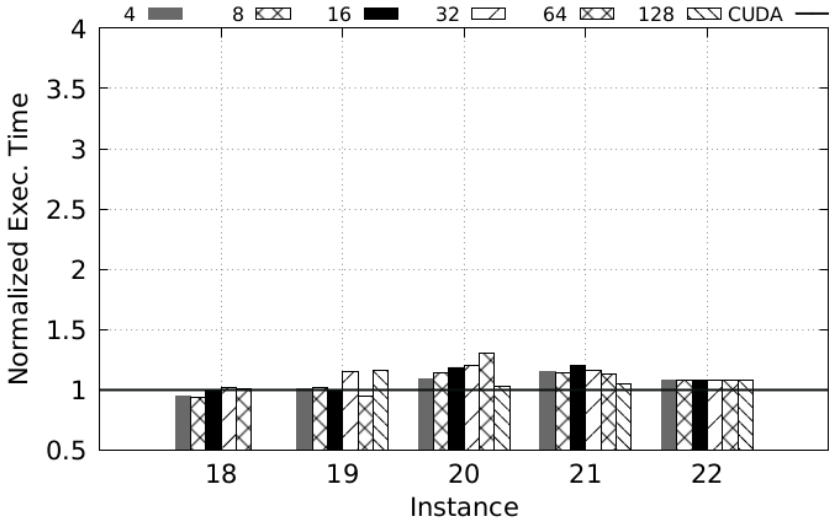

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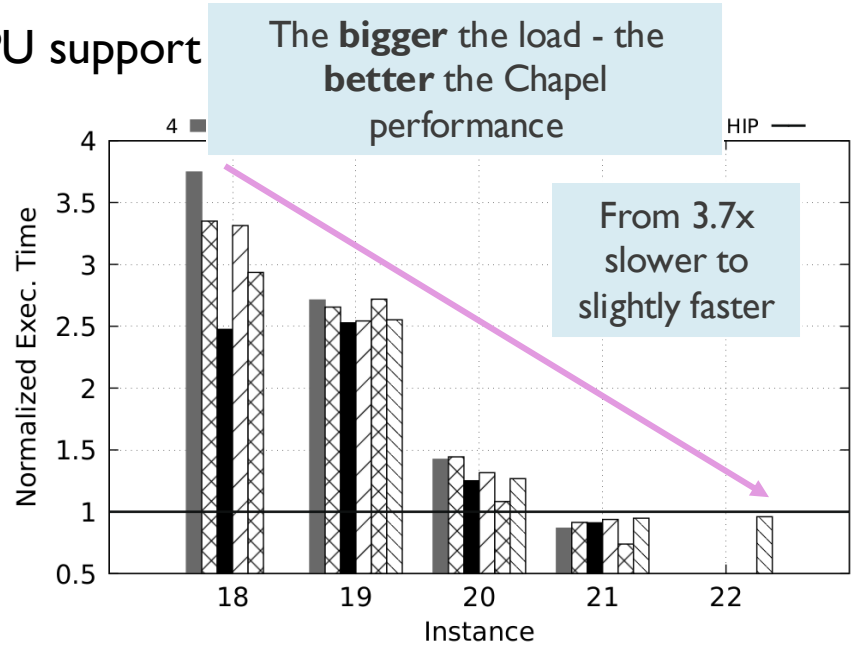


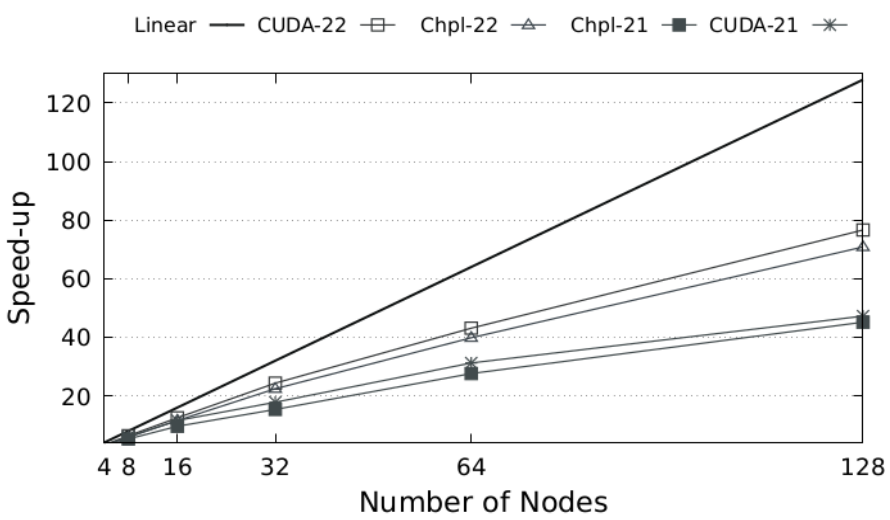
(b) vs. HIP - AMD-based System

imec

Performance Results

Strong Scaling

- N-Queens of sizes N=21 and N=22
- 4-128 computer nodes, speedup compared to the Baseline



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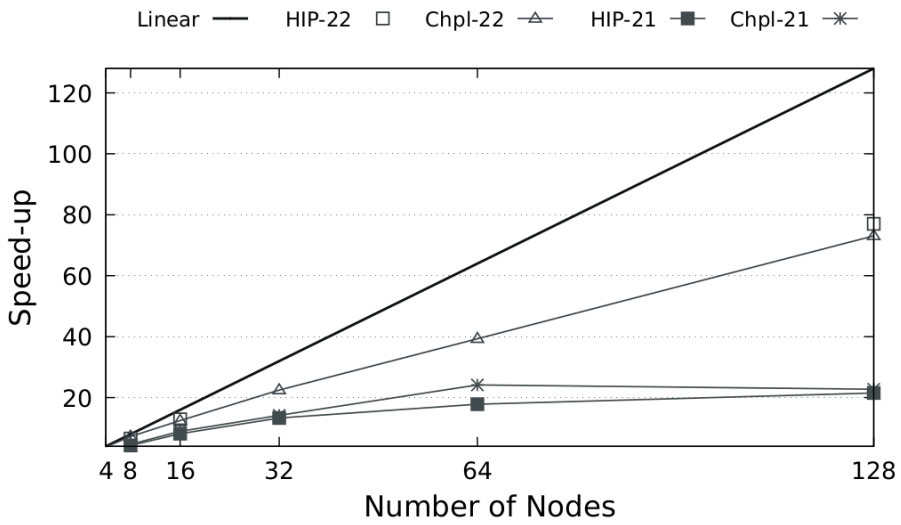


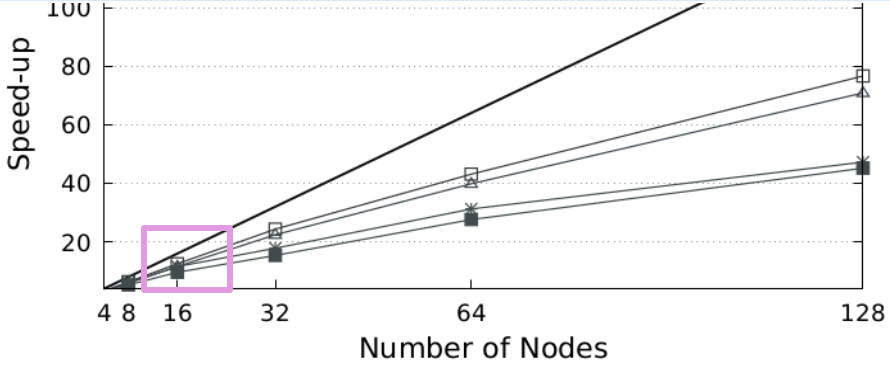
(b) AMD-based system

Performance Results

Strong Scaling

- N-Queens of sizes N=21 and N=22
- 4-128 computer nodes, speedup compared to the Baseline

Load is tiny for 512 GPUs:
Hybrid CUDA 72% *vs.* **Chapel** 60%
of the **linear speedup** on 16 nodes (64 GPUs)



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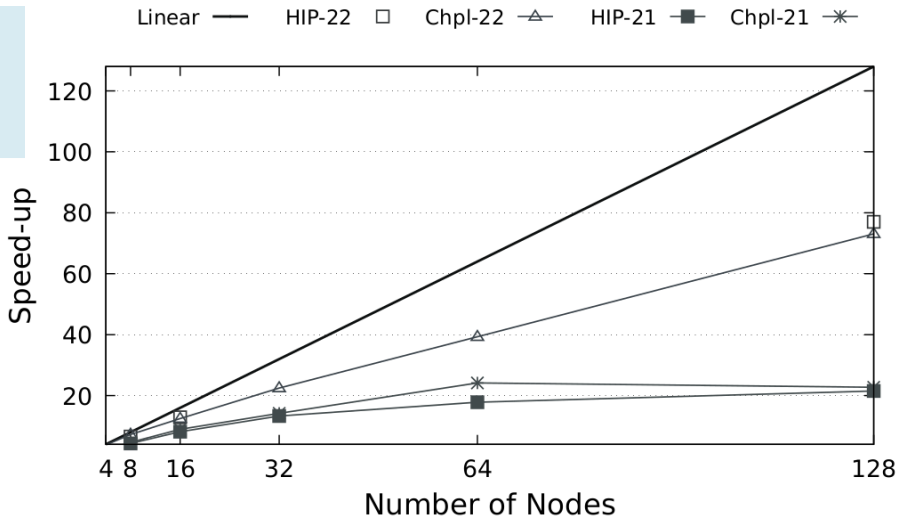

(b) AMD-based system

Performance Results

Strong Scaling

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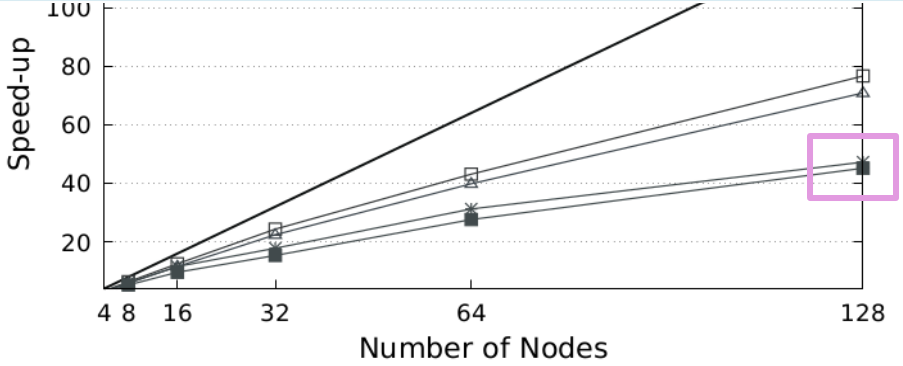
Load is tiny for 512 GPUs:
Drops to **37%** *vs.* **35%**
of the **linear speedup** on **128** nodes (**512** GPUs)



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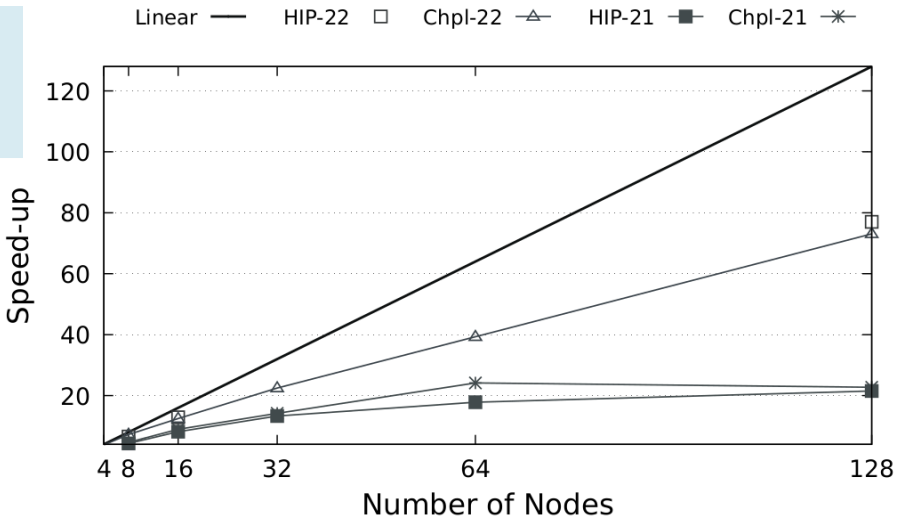

(b) AMD-based system

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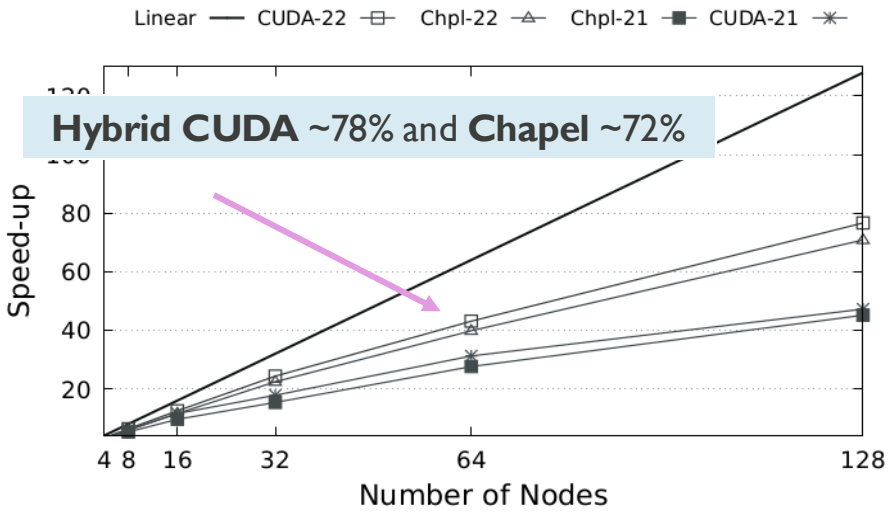

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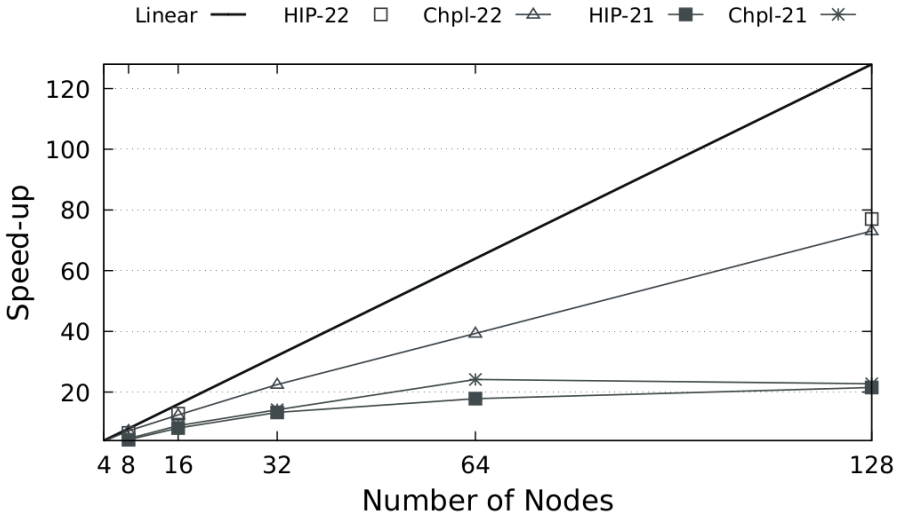

(b) AMD-based system

Performance Results

Strong Scaling

- N-Queens of sizes N=21 and N=22
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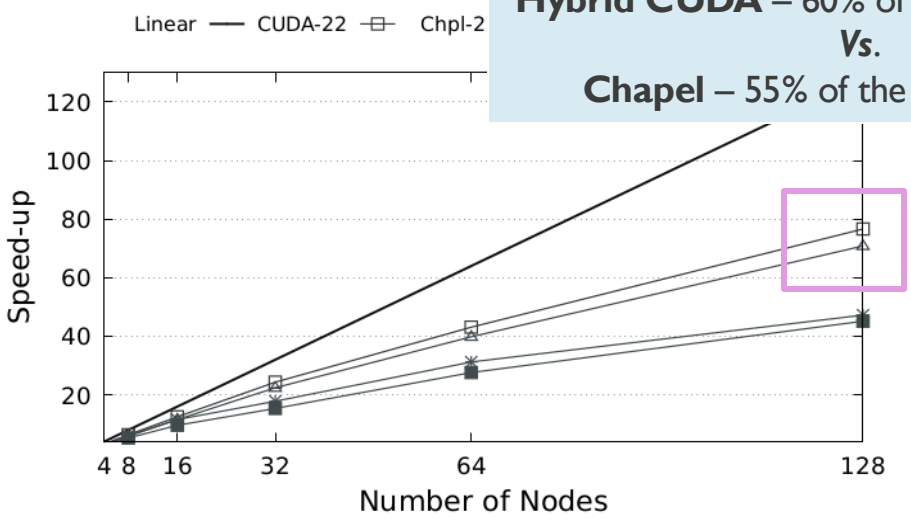
Hybrid CUDA – 60% of the linear speedup
Vs.
Chapel – 55% of the linear speedup



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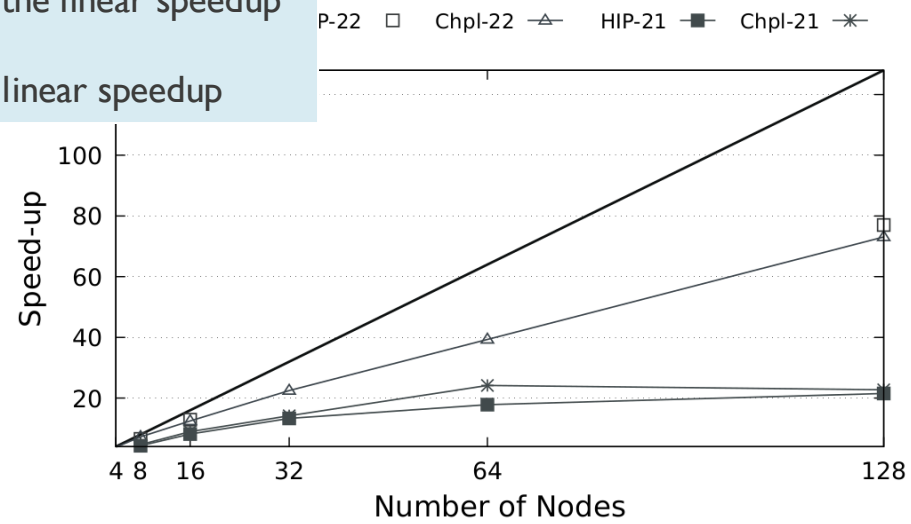

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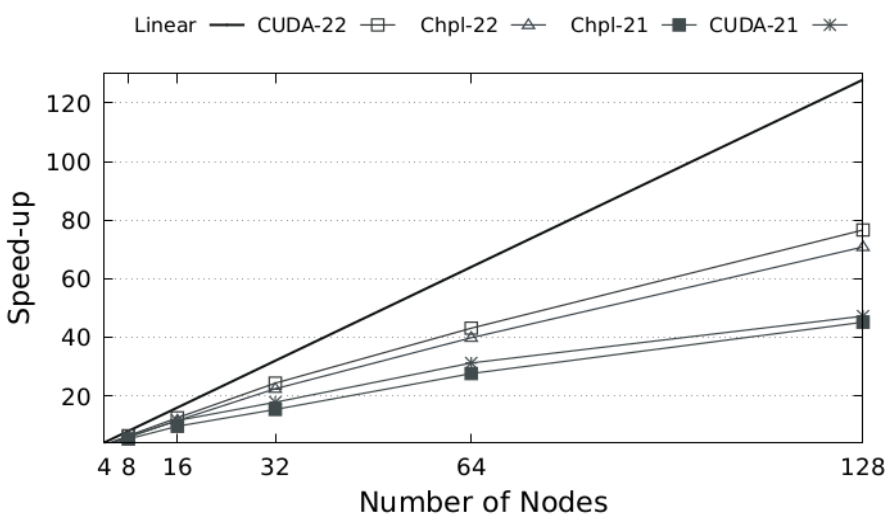

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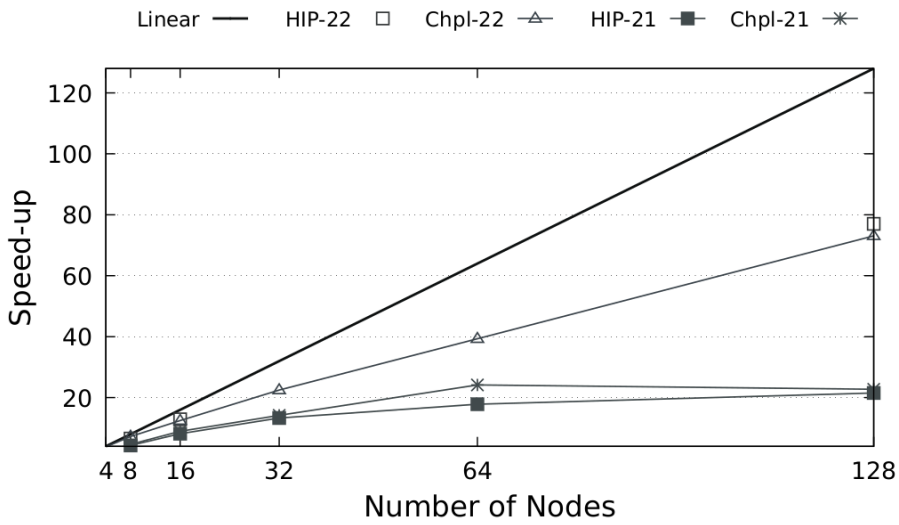

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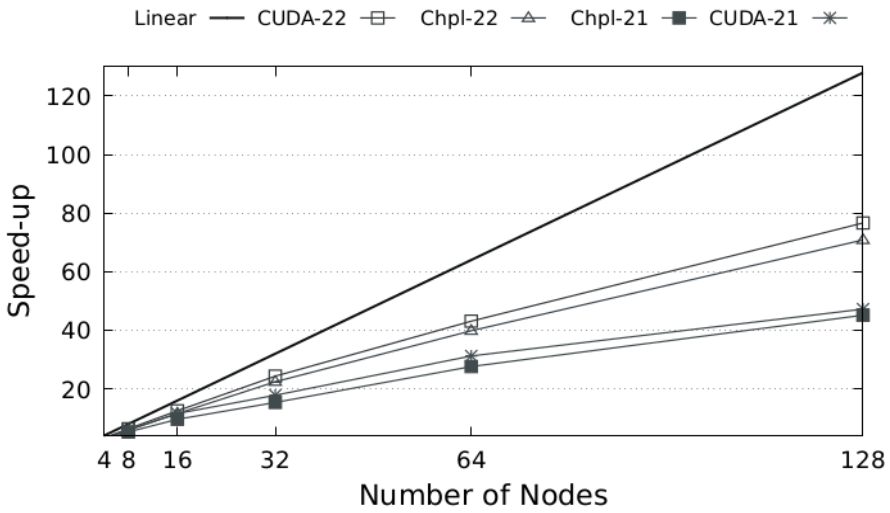

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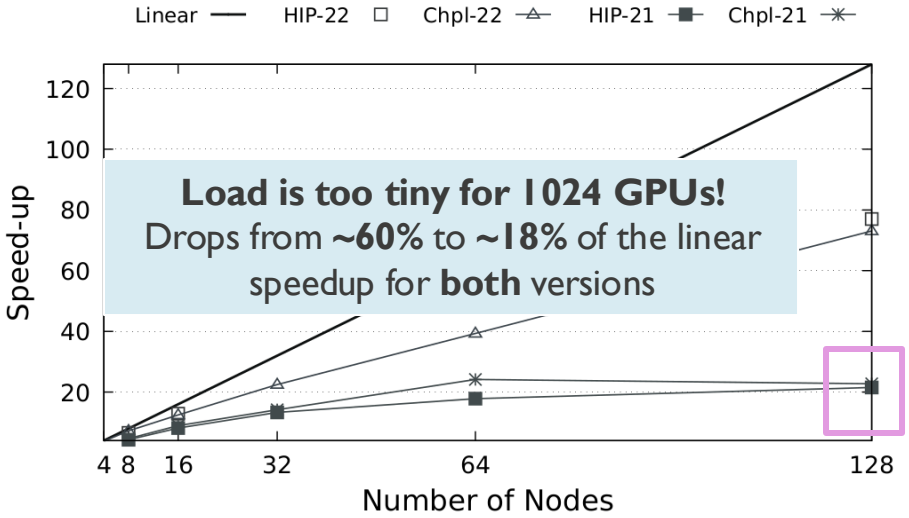

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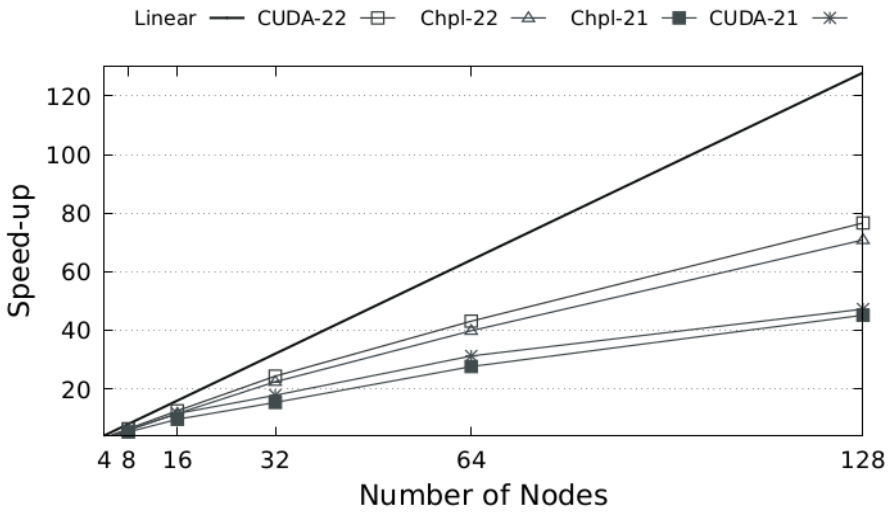

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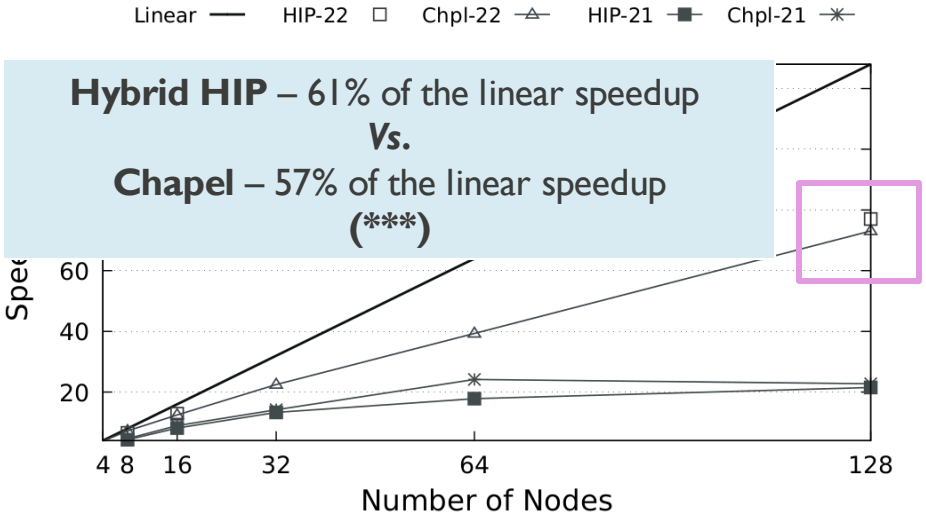

Hybrid HIP – 61% of the linear speedup

Vs.

Chapel – 57% of the linear speedup

(***)

(b) AMD-based system

Research Questions

1. Is it possible to achieve both code and performance portability in distributed tree-based search with Chapel's native GPU support?
    1. **Yes!**
    2. **Minor performance loss** on NVIDIA GPUs and equivalent performance on AMD for big problems.
    3. **Chapel scales similarly** on both systems – up to 128 nodes.

Programming Effort

Programming Effort

Single-node – Multi-GPU

- The HIP, CUDA and Chapel-GPU applications are equivalent in terms of SLOC
  - Single-node – Multi-GPU
  - One thread per GPU
  - N-Queens kernel

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- **Chapel-GPU:** the benefit is to get rid of both HIP and CUDA applications
  - Low/no performance loss for the medium/big problems

Programming Effort

Single-node – Multi-GPU

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  - Single-node – Multi-GPU
  - One thread per GPU
  - N-Queens kernel
- **Chapel-GPU:** the benefit is to get rid of both HIP and CUDA applications
  - Low/no performance loss for the medium/big problems
  - Only one application

Programming Effort

Distributed

- Replacing one hybrid version (CUDA or HIP) with Chapel's native GPU support results in an application 30% shorter.
  - Getting rid of both interoperability codes (CUDA and HIP wrappers) results in a final code 65% shorter.

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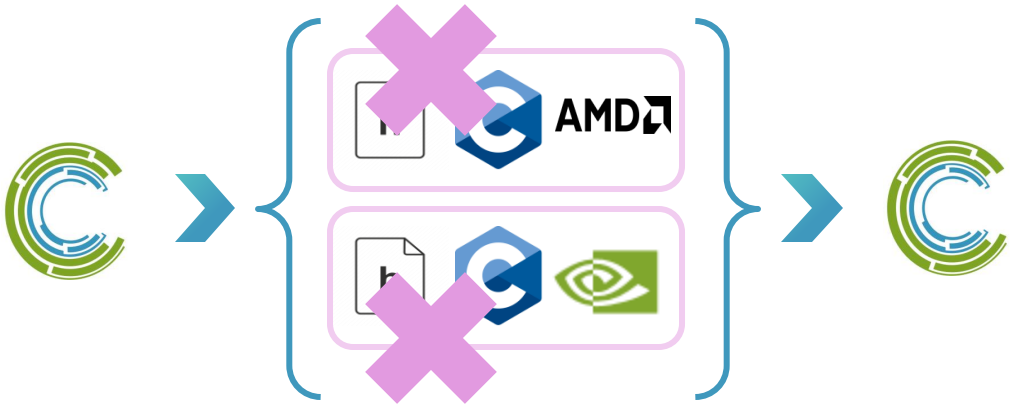
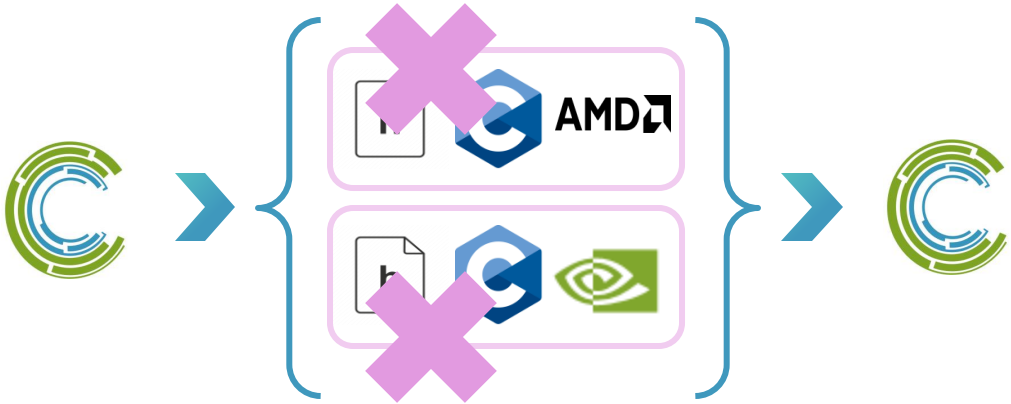


Programming Effort

Distributed

- Replacing one hybrid version (CUDA or HIP) with Chapel's native GPU support results in an application 30% shorter.
  - Getting rid of both interoperability codes (CUDA and HIP wrappers) results in a final code 65% shorter.
  - Only one kernel version to keep
  - Almost no performance loss for distributed execution - biggest loads



Research Questions

1.

2. Is it worth in terms of programming effort?
   1. **Yes!**
   2. **Single-node:** a single application for two different vendors
   3. **Distributed:** getting rid of the kernels and its wrappers results in a much shorter application – small performance loss

Conclusions and Perspectives

Conclusions

- Chapel efficiently unifies the different parallel levels of GPU-powered clusters: inter-node and intra-node (CPUs and GPUs).
  - This allows one to holistically deal with the two major challenges of exascale computing in a unified/productive way:
    - Intra-node and inter-node scalability
    - GPU-aware heterogeneity

Conclusions

- The Chapel-GPU *vs.* its hybrid distributed counterparts achieved:
  - Similar parallel performance
  - Similar strong scaling efficiency on 128 nodes.
- It is possible to achieve both code portability and performance portability in distributed tree-based search with Chapel's native GPU support.
- Using Chapel's Native GPU support instead of interoperability results in a distributed application 65% shorter.

Conclusions

- The main benefit Chapel brings: the **incremental parallelism**:
  - Consider the scenario when the application is developed from scratch.
    - **A first version would likely be written for CPUs**:
      - Serial then multicore
    - **From multicore to distributed:**
      - Due to the unified memory model (PGAS), a distributed application in Chapel can be very similar to its multicore counterpart.
    - **From CPU to GPU:** how to write and compile the mix of OpenMP+CUDA or MPI+CUDA?
- In Chapel, all these steps are significantly easier than other paradigms:
  - One language for CPUs, GPUs, single-node and distributed computing
  - No mix of programming models

Perspectives

- Study the generated target code to better understand the results
- **From the N-Queens to Combinatorial Optimization Problems**:
  - Branch-and-Bound search instead of distributed Backtracking
  - Variants of the N-Queens, FSP, VRP, MinLA, etc.
    - (e.g.; FSP Ta057 ~30-years PFSP instance)
  - Checkpointing for solving to the optimality larger problems
- More efficient ways of exploiting intra-node parallelism?
  - The present algorithm was conceived for small-sized clusters
  - Is there a more efficient way of exploiting intra-node parallelism?
    - One locale/sublocale per GPU?
    - Is it possible to use all GPUs/CPU cores to decrease execution time?

Acknowledgments

- This work was supported by the Ministry of Education, Youth and Sports of the Czech Republic through the e-INFRA CZ (ID:90254) -- Project EU2022D08-197.
- It is also supported by the Agence Nationale de la Recherche (ref.ANR-22-CE46-0011) and the Luxembourg National Research Fund (ref. INTER/ANR/22/ 17133848), under the UltraBO project.
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Thank you!

Questions?

https://github.com/tcarneirop/ChOp

Chapel-based Optimization on Github

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imec
embracing a better life